Master’s thesis or research internship in collaboration with Fraunhofer Institute AISEC

Design of a High-Performance Hardware Security Module

Abstract
This thesis or internship is part of a project on an integrated hardware security module for a high-performance system on chip. The precise scope of this work will be determined individually based on the personal experience and interests.

Requirements:
- Strong background in Computer Architecture
- Background in Hardware Security
- Experience with VHDL, Verilog or System Verilog
- Creativity and Independent Work Style
- Background in Real-Time Operating Systems preferred
- C and Assembler Programming Skills preferred
- Background in ASIC Design preferred

Date: 02.11.2017
Start: any time

Contact
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